James Mackenzie

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PROFILE

James Mackenzie is a silicon engineering leader who has a track record of delivering first time right silicon and systems. He has consistently exceeded employers' needs and expectations with his ability to quickly and efficiently understand, lead, and deliver complex cross-team projects.

James has proven his ability to lead and grow teams while adeptly troubleshooting and resolving complex technical issues. At Microsoft, he currently leads the AI Silicon Engineering SoC teams responsible for DV Test Content, emulation, and validation as well as defining and driving AI Silicon's relationship with internal SW and FW teams. At Intel, he led the NVMe subsystem verification team targeting the next generation of enterprise and client SSDs; in earlier roles at Intel he worked on block level design and verification. Prior to those roles, James worked at IBM in a software engineering role, where he was a member of a multinational team developing a high-value consumer-facing software product. He has also worked at Wind River, where he designed and developed a number of internal tools for Wind River Education Services.

SKILLS

Languages:	Python, C, C++, SystemVerilog.
Software:	Synopsys VCS/Design Compiler, Git.
Hardware:	Synopsys ZeBu, Cadence Palladium.

WORK EXPERIENCE

Director, Design Verification, Microsoft; Mountain View, CA, USA
March 2020-Present

- Simultaneously led and managed the SoC Test Content functional verification team and the emulation team in AI Silicon Engineering (AISiE), aligning overall strategy to ensure A0 production readiness.
- Owned AISiE's relationship with SW/FW partner teams to align design readiness with software, successfully enabling the production software stack and workloads on emulation and silicon bringup platforms and ensuring power, performance, and functionality were debugged and optimized through pre-silicon and post.
- Owned multiple external relationships with EDA tool vendors and successfully led proofs-of-concepts and negotiations that realized significant cost and time savings.
- Developed test generation and checking methodologies that were seamlessly portable across pre-silicon, emulation, and post-silicon environments.
- Worked with internal and external validation, platform, system integration, and silicon screen teams to solve failures and develop debug and test methodologies to ensure success at datacenter scale.

Design Verification Engineer, Intel; Vancouver, BC, Canada
May 2014-August 2014 & May 2013-December 2013 (Intern); January 2016-February 2020

- Led a cross-site NVMe subsystem functional verification team, providing day-to-day technical leadership and guidance to team members while balancing quality and schedule requirements.
- Designed and oversaw the implementation of a multi-UVC subsystem level test environment.
- Verified multiple RTL designs from a blank-slate UVC and test plan to 100% coverage closure using SystemVerilog and UVM at both block level and protocol level.
- Developed methodologies and internal verification IP to improve productivity and effectiveness, with these efforts recognized division-wide.

- Mentored and supervised new team members and successfully ramped them into productive members of the ASIC design and verification team.
- Developed and maintained RTL designs from initial planning to post-tapeout.
- Successfully prepared RTL designs for delivery using Spyglass and Design Compiler.
- Gained significant in-depth experience in SSD architecture, specifically in NVMe over PCIe.

Software Development Intern, IBM; Victoria, BC, Canada
September 2012-December 2012
- Fixed defects in and added new features to a major consumer-facing Java-based IBM product.
- Participated as a member of an international team in a challenging and rewarding environment.
- Created automated JUnit test suites in preparation for a major product release.

Software Development Intern, Wind River Systems; Ottawa, ON, Canada
January 2012-April 2012
- Developed a number of subsystems for an internal automated GUI testing system using Python and Qt.
- Led the design and development of an internal file sharing website using Python, PHP, HTML, and CSS. The system was successfully deployed on multiple servers around the world and was capable of automatically ensuring file redundancy and availability.
- Engineered an online dashboard in PHP that allowed engineers to see how customers rated their work.

EDUCATION

B.Eng, Computer Engineering, University of Victoria. Specialization in Embedded Systems.

PUBLICATIONS AND PROJECTS

DatagenDV: Python Constrained Random Test Stimulus Framework; DVCon — 2023
Co-authored a paper on DatagenDV, a Python framework for generating C compatible test stimulus using YAML and random constraints. The framework leveraged multiple open-source projects and was similarly contributed to the open-source DV community. DV test development timelines were shown in the paper to be significantly reduced by DatagenDV's ability to leverage existing SystemVerilog constraints from block testbenches. The paper was presented orally at DVCon 2023.

Little Dog; University of Victoria — 2015
The major term project of CENG 441 (Design of VLSI Systems), with team members from CENG 499 (Design Project II) and MECH 400 (Design Project). Led development and testing of a number of internal blocks for an FPGA-based PD control system for a quadruped rover using VHDL. Also led integration and verification efforts of the overall design using ModelSim. Awarded the Design Technical Project Award by the IEEE Victoria Chapter out of 30 teams.

Third Eye; University of Victoria — 2015
The major term project of CENG 490 (Design Project II). Led development and hardware engineering of a blind spot traffic detection system for cyclists. Made use of ultrasonic sensors, an Arduino, and BLE to communicate traffic data to an iPhone. The iPhone app allowed users to listen to their own music while traveling, as the app would lower the volume of the music or play an alert if a threat was closing on them depending on the threat's closing speed and distance. Awarded the Design Technical Project Award by the IEEE Victoria Chapter out of 15 teams.

ACTIVITIES AND INTERESTS

Motorsport, photography, hiking, English literature, quantum physics, public speaking, mentorship, and leadership.